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Low Power Consumption Complementary Inverters with n-MoS_2 and p-WSe_2 Dichalcogenide Nanosheets on Glass for Logic and Light-Emitting Diode Circuits

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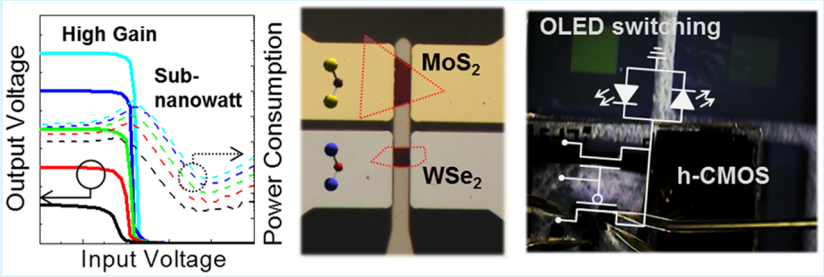
Supporting Information



ABSTRACT: Two-dimensional (2D) semiconductor materials with discrete bandgap become important because of their interesting physical properties and potentials toward future nanoscale electronics. Many 2D-based field effect transistors (FETs) have thus been reported. Several attempts to fabricate 2D complementary (CMOS) logic inverters have been made too. However, those CMOS devices seldom showed the most important advantage of typical CMOS: low power consumption. Here, we adopted p-WSe_2 and n-MoS_2 nanosheets separately for the channels of bottom-gate-patterned FETs, to fabricate 2D dichalcogenide-based hetero-CMOS inverters on the same glass substrate. Our hetero-CMOS inverters with electrically isolated FETs demonstrate novel and superior device performances of a maximum voltage gain as ~27, sub-nanowatt power consumption, almost ideal noise margin approaching $0.5V_{DD}$ (supply voltage, V_{DD} = 5 V) with a transition voltage of 2.3 V, and ~800 μs for switching delay. Moreover, our glass-substrate CMOS device nicely performed digital logic (NOT, OR, and AND) and push−pull circuits for organic light-emitting diode switching, directly displaying the prospective of practical applications.

KEYWORDS: *complementary inverter, MoS_2, WSe_2, glass, sub-nanowatt, high gain*

INTRODUCTION

After graphene,[1,2] two-dimensional (2D) semiconductor materials with discrete bandgap have attracted much attention from many researchers, owing to their interesting physical properties and potentials for future nanoscale electronics.[3−35] Like graphene, those 2D semiconductors are formed by mechanical exfoliation using scotch tapes in general, so that those are called nanosheet or nanoflake. Among many nanosheet materials, molybdenum disulfide (MoS_2)[9−24] and tungsten diselenide (WSe_2)[23−35] are known as pacesetting materials, because they have displayed excellent carrier mobility, high on/off current ratio, and good sub-threshold swing in a field-effect transistor (FET) form as 2D n- and p-type channels, respectively. In fact, 2D WSe_2 has been found ambipolar, so that researchers might even report complementary-like inverters[26,27] using such ambipolar properties; this WSe_2 played as both n- and p-channel depending upon the contact metal,[25−34] chemical doping in the channel,[27−29] and the polarity of applied gate voltages.[30−34] However, the homogeneous 2D WSe_2 complementary inverter with chemical doping[27] shows relatively unstable behavior in air ambience, because the chemical doping for n-type activity could not be supportive for ambient stability. It means that the n-type doping is difficult and probably not matched to the nature of exfoliated 2D WSe_2, which is slightly closer to p-type than to n-type. Another type of homogeneous complementary inverter, comprised of dual-gate WSe_2 FETs,[26] always required additional gate biases to adjust channel polarities and threshold voltages. Therefore, many researchers have rather attempted to fabricate homogeneous 2D inverters of depletion-load type[7−11] than complementary inverters, although depletion-load inverters should be inferior to the complementary inverter with respect to power dissipation and voltage gain. Recently, several efforts to fabricate stable heterogeneous complementary-like (hetero-CMOS) inverters with two different channel materials, among which one-dimensional (1D)−2D hybrid channels[15,35] and 2D−2D heterogeneous dichalcogenide channels[21−23] are found. However, until now, such 2D−2D dichalcogene-based

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CMOS inverters, which would be the most natural in device form, are still a few and display so primitive performances without reporting such important basics as power consumption and dynamic switching. In particular, we may hardly find any power consumption data yet from 2D−2D CMOS reports (see details in Table S1), although low power consumption is the most important advantage of the CMOS inverter over single-FET-type inverters.

Here, we adopted WSe_2 and MoS_2 nanosheets for separate p- and n-channels using a direct imprint method,[15−18,24] to fabricate 2D dichalcogenide-based hetero-CMOS inverters not only on SiO_2/p^+-Si but also on a glass substrate. Our hetero-CMOS inverters with bottom-gated p- and n-FETs well operate particularly on a glass substrate, demonstrating novel and superior device performances of a maximum voltage gain as ∼27, sub-nanowatt power consumption in switching, almost ideal noise margin approaching $0.5V_{DD}$ (supply voltage, V_{DD} = 5 V) with a transition voltage of 2.3 V, and ∼800 μs for switching time. Likewise, satisfying most of the important CMOS properties, our glass-substrate CMOS device performed digital logic (NOT, OR, and AND) and push−pull circuits for organic light-emitting diode (OLED) switching.

EXPERIMENTAL SECTION

Device Fabrication. First of all, two kinds of gate dielectrics were prepared: (i) thermal oxidized 285 nm thick SiO_2 on heavily doped p^+-Si wafer as the universal gate and (ii) atomic-layer deposited (ALD) 50 nm thick Al_2O_3 on a gate-patterned 25/25 nm thick Au/Ti bilayer electrode (Ti was always deposited prior to Au as a result of its better adhesion to glass). As the next step, a direct imprint method[15−18,24] was implemented, as described in panels a−e of Figure S1, to transfer two different kinds of nanosheets on target places. A MoS_2 nanosheet was mechanically exfoliated using a sticky polydimethylsiloxane (PDMS) stamp from single-crystal bulk MoS_2 (see Figure S1a). The PDMS stamp with exfoliated MoS_2 was transferred onto a quartz plate, and the quartz plate with our MoS_2 nanosheet was flipped over and moved to be aligned on previously prepared two kinds of substrates that had already been mounted on the stage of a charge-coupled device (CCD)-equipped microaligner, as shown in Figure S1b. The MoS_2 nanosheet was then precisely attached on a gate dielectric by controlling the motion of the microaligner stage for van der Waals force, being monitored by the CCD image. Figure S1c illustrates the MoS_2 nanosheet stacked on SiO_2 or Al_2O_3 gate dielectrics by van der Waals force. A 25/25 nm thick Au/Ti electrode was patterned for ohmic source/drain (S/D) contact with a n-channel MoS_2 nanosheet (Ti was always deposited prior to Au as a result of its work function matching with MoS_2).[17] The same attachment processes were carried out to transfer and attach the WSe_2 nanoshseet close to the MoS_2 nanosheet FET (see Figure S1d). Sequentially, 50 nm thick Pt electrode, which is known to have a ∼5.5 eV work function, was patterned to make low-resistance contact with a p-channel WSe_2 nanosheet, as shown in Figure S1e. Both the metal electrodes of Au/Ti and Pt were patterned by photolithography and lift-off method and were deposited by a direct current (DC) magnetron sputtering system in a high-vacuum chamber of $\sim 10^{-7}$ Torr. After completion of electrical measurements of the unencapsulated complementary inverter, 200 nm thick fluoropolymer CYTOP (Asahi glass, CTX-809M) was stacked by the spin-coating method on top, followed by curing at 100 °C for 30 min.

For the push−pull circuit operation, the output terminal of CYTOP-encapsulated complementary inverter was interconnected by Au wiring with two antiparallel green (λ ∼ 560 nm) OLEDs (respective light-emitting area of 2 × 2 mm^2), which were manufactured from Samsung Display.

Electrical Measurements. All electrical measurements were performed in the dark with a semiconductor parameter analyzer (Agilent 4155C) and function generator (Tektronix AFG3022B).

RESULTS AND DISCUSSION

Hetero-CMOS on SiO_2/p^+-Si. Figure 1a displays the hetero-CMOS processes on a 285 nm thick SiO_2/p^+-Si

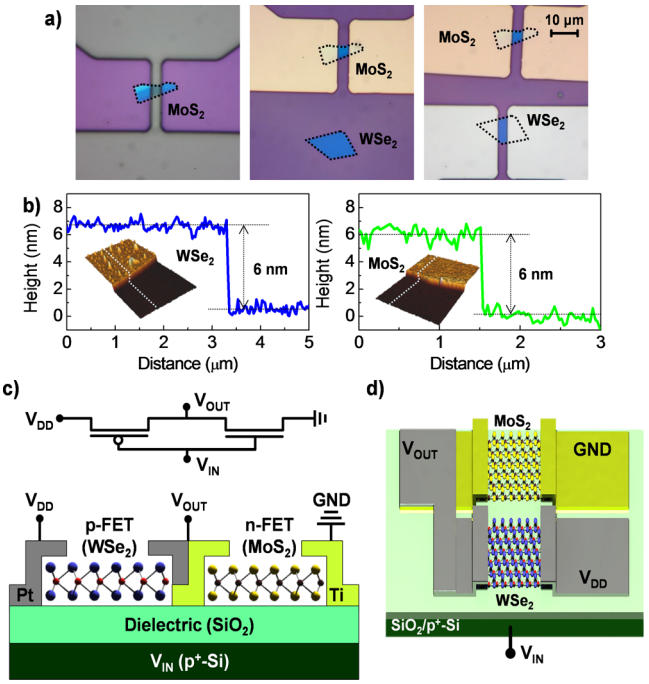

Figure 1. (a) Optical microscopic images displaying device fabrication processes, which were implemented on a 285 nm thick SiO_2/p^+-Si wafer using the direct imprint method. The left image indicates a MoS_2 nanosheet along with ultraviolet (UV)-patterned photoresist prior to Au/Ti S/D deposition, while the central image shows a fabricated n-MoS_2 FET and a direct imprint-transferred WSe_2. The right image displays fabrication-completed n- and p-FETs. (b) Line profiles and topographic images of (left) WSe_2 and (right) MoS_2 nanosheets as obtained from AFM. (c and d) Schematic circuit diagram, cross-section, and 3D image illustrating the hetero-CMOS inverter on a 285 nm thick SiO_2/p^+-Si universal gate.

universal gate. After finding a 6−7 nm thin exfoliated MoS_2, an Au/Ti S/D electrode was patterned by photolithography and lift-off processes. Then, a WSe_2 nanosheet of about the same thickness was transferred near a MoS_2 sheet by the direct imprinting method,[15−18,24] followed by Pt electrode patterning for S/D contact [see the atomic force microscopy (AFM) results in Figure 1b for the respective thickness profiles and images of MoS_2 and WSe_2]. These two FETs are connected in series to function as a CMOS inverter couple, as shown in the schematic cross-section and three-dimensional (3D) views of panels c and d of Figure 1.

Electrical Performances of Hetero-CMOS on SiO_2/p^+-Si. The electrical properties of our individual 2D FET with p-WSe_2 and n-MoS_2 channels on the universal gate are introduced in panels a and b of Figure 2. According to the transfer curves (drain current−gate voltage, I_D-V_{GS}) of p- and n-FETs, 2D WSe_2 FET shows an order of magnitude higher on-current than that of MoS_2 FET, also displaying more desirable behavior with respect to the threshold voltage (V_{TH} = −10 V for n-FET and +1 V for p-FET, as shown in panels d and e of Figure S2). Therefore, our bottom-gate FET architecture apparently operates better for WSe_2 than MoS_2 nanosheet, promising a higher mobility from p-FET. Output curves (drain current−drain voltage, I_D-V_{DS}) of FETs display in Figure 2c

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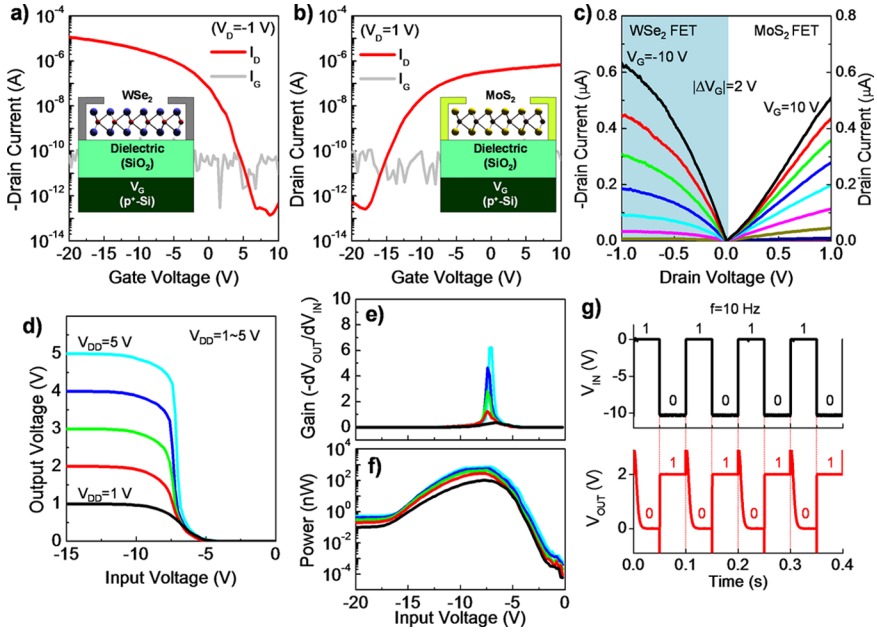

Figure 2. Drain current−gate voltage (I_D−V_{GS}) transfer curves of universal gate FETs using (a) p-channel WSe_2 and (b) n-channel MoS_2 nanosheets as obtained from $|V_{DS}|$ = 1 V (see the respective insets for schematic cross-sections of p- and n-FETs). (c) Drain current−drain voltage (I_D−V_{DS}) output curves of universal gate FETs using p-channel WSe_2 and n-channel MoS_2 nanosheets in a gate voltage range of V_{GS} from −10 to 10 V with 2 V steps. (d) Voltage transfer characteristics (V_{IN}−V_{OUT}), (e) voltage gains ($-dV_{OUT}/dV_{IN}$), and (f) power consumptions ($P = I_{DD}V_{DD}$) of hetero-CMOS on the wafer substrate as obtained under various supply voltages (V_{DD} values) ranging from 1 to 5 V. (g) Dynamic output voltage response obtained from square wave input of 0 and −10 V at 10 Hz under V_{DD} = 2 V.

that Au/Ti and Pt electrodes are working well for ohmic contacts to n- and p-channels, respectively. Interestingly, the output curves of p-FET show quite a saturation behavior, while those of n-FET display linear behavior. This means that the p-FET with 2D WSe_2 tends to readily saturate unlike the n-FET with the similarly thin MoS_2. We attribute this behavior to any unique materials characteristic of 2D WSe_2. The saturation mobility (μ_{sat}) of p-FET was estimated to be ∼4 $cm^2\ V^{-1}\ s^{-1}$ (linear mobility, μ_{lin} ∼ 100 $cm^2\ V^{-1}\ s^{-1}$), and n-FET shows only ∼1.2 $cm^2\ V^{-1}\ s^{-1}$ for its linear mobility (μ_{lin}) (see the respective plots of panels a−c of Figure S2), when we used two different mobility eqs 1 and 2 shown below.[36]

$$\mu_{sat} = \frac{2}{C_{OX}}\frac{L}{W}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \quad \text{for saturation mobility} \tag{1}$$

$$\mu_{lin} = \frac{1}{V_D C_{OX}}\frac{L}{W}\frac{\partial I_D}{\partial V_{GS}} \quad \text{for linear mobility} \tag{2}$$

CMOS inverter circuit on the universal gate resulted in the voltage transfer characteristics (VTCs) of Figure 2d, which was obtained under various supply voltages (V_{DD} values) ranging from 1 to 5 V. Because our n-MoS_2 FET was in quite a depletion mode, our hetero-CMOS inverter displays a very negative transition voltage at −7.5 V, along with a maximum voltage gain ($-dV_{OUT}/dV_{IN}$) of ∼6 in Figure 2e. Moreover, this device shows a broad range of peak power consumption ($P = V_{DD}I_{DD}$) during high−low switching (Figure 2f), which originates from unpatterned gate structure (Figure 1c). The peak power consumption appears as large as ∼1 μW. Dynamic inverter switching using 0 and −10 V input (V_{IN}) was demonstrated at 10 Hz under V_{DD} of 2 V in Figure 2g, but it began to show over-/undershoot of output voltage (V_{OUT}) at 10 Hz (along with 10 ms delay) as a result of overlap capacitance-induced booster effects.[24,37,38]

Electrical Performances of Hetero-CMOS on Glass. To remove such undesirable effects from an unpatterned universal gate as large power consumption, low voltage gain, and switching speed limit along with V_{OUT} overshoot,[24,37,38] we fabricated a patterned bottom-gate hetero-CMOS inverter on a glass substrate. Figure 3a shows our hetero-CMOS inverter fabrication processes on glass, which was basically the same as those on the SiO_2/p^+-Si substrate, except the gate metal (Au/Ti) was patterned on glass prior to atomic layer deposition (ALD) of 50 nm thick Al_2O_3 dielectric. As shown in the central photo image zoomed from our CMOS device on glass, there is still a little gate/source overlap area in our FETs and the central device image is schematically described in Figure 3c. In this hetero-CMOS couple with two FETs, the MoS_2 thickness was 3 times larger than that of WSe_2 (∼7 nm) (Figure 3b). According to the transfer curves of p- and n-FETs on glass (panels d and e of Figure 3, respectively), a few times higher on-current I_D is achieved from p-FET with 2D WSe_2 approaching 10 μA at −5 V of gate bias. Both FETs show negative threshold voltages of −1.3 V for p-FET and −1 V for n-FET (see the respective plots of panels f and g of Figure S3). Field effect mobilities were estimated on the basis of the transfer curves but also the output curves of the two FETs in panels a and b of Figure S3. Although the output curves of p-FET somewhat contain saturation behavior, we calculated both of its linear (∼16 $cm^2\ V^{-1}\ s^{-1}$) and saturation (∼7 $cm^2\ V^{-1}\ s^{-1}$) mobilities. The linear mobility is ∼10 times higher than that of n-FET (1.6 $cm^2\ V^{-1}\ s^{-1}$) according to the respective plots of panels c−e of Figure S3. The gate leakage current from both p- and n-FETs on glass displayed a much desirable level of ∼100 fA, which is 3 orders of magnitude lower than that from FETs on wafer (∼100 pA). It is because the gate-patterned CMOS on glass has a much

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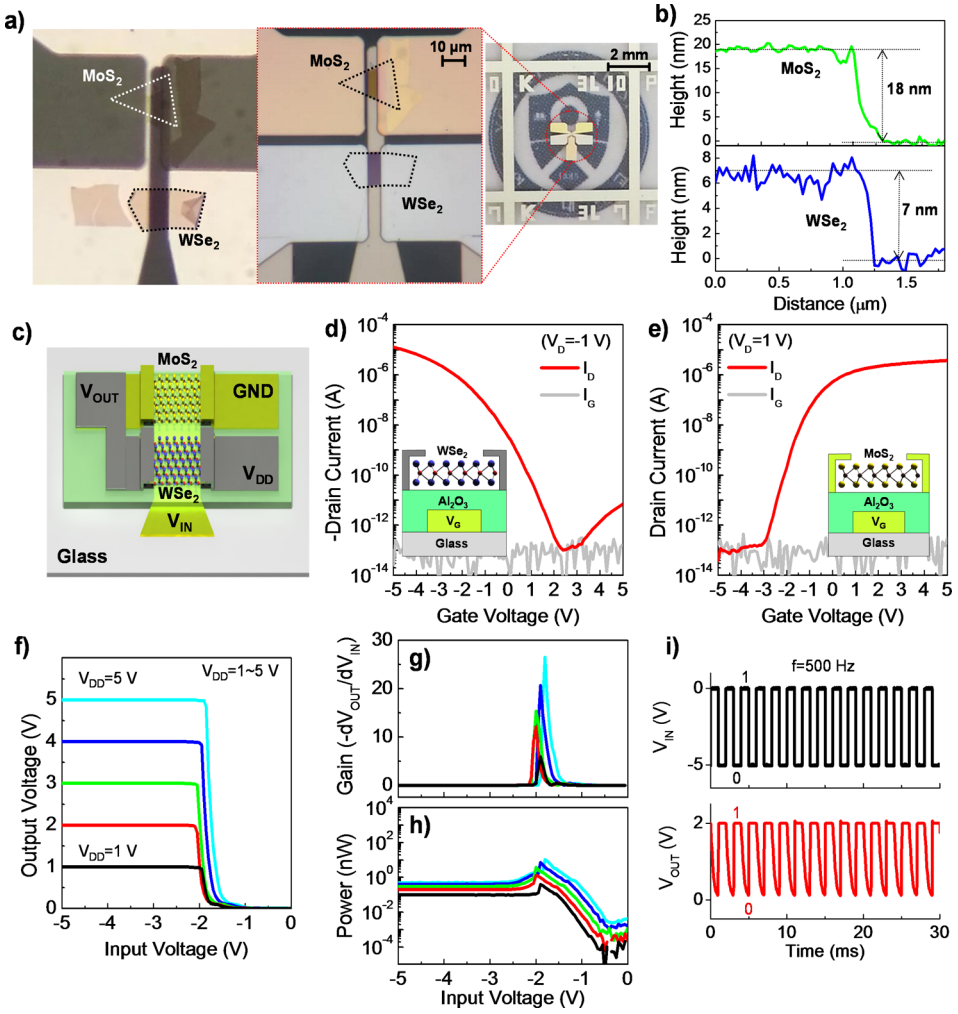

Figure 3. (a) Left optical image was taken under bottom illumination through glass during the fabrication process, indicating the patterned bottom-gate, completed MoS_2 FET and transferred WSe_2 flake. The central image indicates a completed hetero-CMOS inverter as another optical image taken using top illumination, while the right image is a snapshot photo image of hetero-CMOS on glass. (b) AFM line profiles of 18 nm thick MoS_2 and 7 nm thin WSe_2 nanosheets. (c) Schematic 3D illustration of hetero-CMOS inverter with a 50 nm thick Al_2O_3 gate. I_D–V_{GS} transfer curves of patterned bottom-gate FETs for (d) p-channel WSe_2 FET and (e) n-channel MoS_2 FET as obtained from $|V_{DS}|$ = 1 V (the respective insets show schematic cross-sections of p- and n-FETs). (f) Voltage transfer characteristics (V_{IN}–V_{OUT}), (g) voltage gains ($-dV_{OUT}/dV_{IN}$), and (h) power consumptions ($I_{DD}V_{DD}$) of hetero-CMOS on a glass substrate were obtained under various supply voltages (V_{DD} values) ranging from 1 to 5 V. (i) Dynamic output voltage responses obtained from square wave input of 0 and −5 V at 500 Hz frequencies under V_{DD} = 2 V.

smaller overlap area between gate/source electrodes. The hetero-CMOS inverter with a patterned gate on glass (see Figure 3c) displays quite an excellent device performance over the previous inverter without gate patterning. According to the VTCs and voltage gain curves of panels f and g of Figure 3, the high−low transition voltage was located near ∼ −2 V and the maximum gain (at V_{DD} = 5 V) appears to be ∼27, which is 4.5 times higher than that of CMOS with a universal gate. Figure 3h dispalys sub-nanowatt power consumption behavior in the static states, which is one of the intrinsic advantages from a complementary inverter. In particular, the peak power was as small as 10 nW but would be less than sub-nanowatt[35,39] during dynamic inverter switching in a small input voltage range (for instance, between −3 and 0 V). We attribute such a small power consumption to the gate patterning, low supply voltage (V_{DD}), and FET device isolation as a result of the hetero-2D CMOS structure. Dynamic switching was carried out at 500 Hz, as shown in Figure 3i; here, we used V_{IN} between −5 and 0 V under a V_{DD} of 2 V. No over-/undershoot phenomena were shown, because the overlap capacitance was much reduced by gate patterning unlike the case of the other device with a universal gate.[24,37,38] A dynamic switching delay of ∼800 μs was observed for 2 V full output signal, somewhat attributed to the overlap capacitance. In fact, it might not be easy to obtain high-quality WSe_2 and MoS_2 nanosheets on Al_2O_3/patterned gate (Au/Ti), which causes the nanosheets to be warped unlike the cases on the flat SiO_2/p^+-Si gate. However, according to AFM results in Figure S4, the surface contour of the patterned Au/Ti electrode structure appears quite safe, showing a very small aspect ratio (∼0.03). Because ALD Al_2O_3 should be conformal on the Au/Ti electrode, the roughness and contour of ALD Al_2O_3 gate dielectric would be almost the same as that of Au/Ti. As a result, our FETs appear working well without any problem.

Hetero-CMOS Modulated Using Thin 2D Nanosheets and CYTOP Layer. Despite the above operation of hetero-CMOS inverter on glass, the device may not be practical yet in terms of logic function, because the device shows negative

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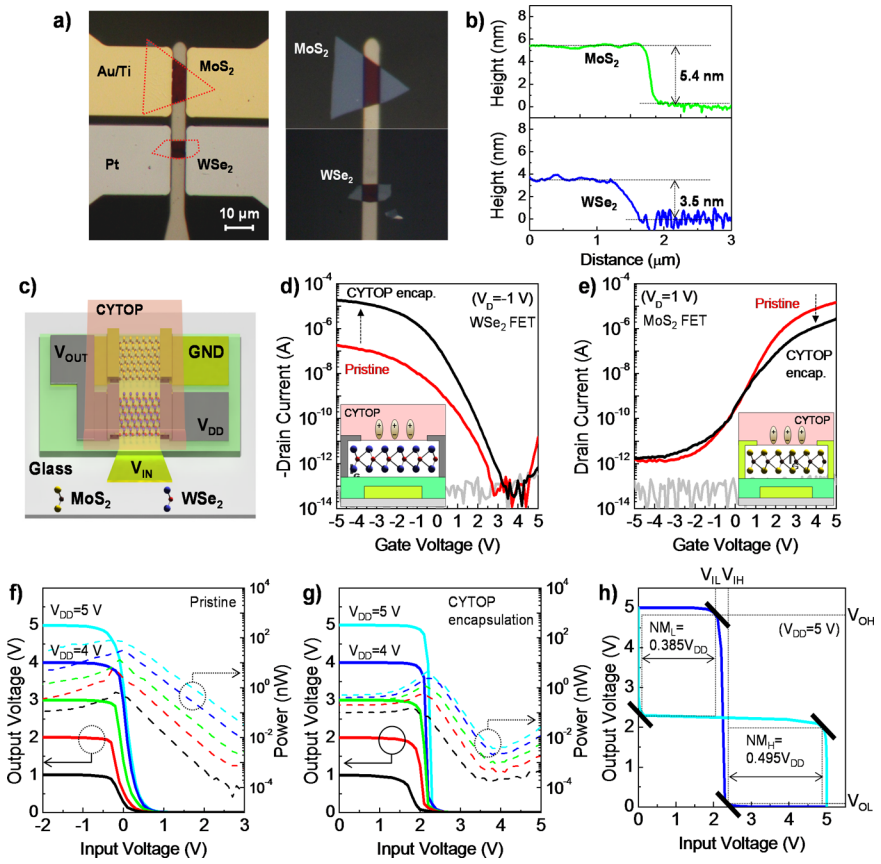

Figure 4. (a) Optical images of (left) completed hetero-CMOS inverter fabricated on glass and (right) just transferred n-MoS_2 and p-WSe_2 nanosheets onto Al_2O_3 gate-insulator/patterned gate. (b) AFM line profiles of 5.4 nm thin MoS_2 and 3.5 nm thin WSe_2 nanosheets. (c) Schematic 3D illustration of hetero-CMOS inverter encapsulated with a fluoropolymer CYTOP layer on top. I_D−V_{GS} transfer curves of patterned bottom-gate FETs for (d) p-channel WSe_2 FET and (e) n-channel MoS_2 FET before and after CYTOP encapsulation. Respective insets show schematic cross-sections of CYTOP-encapsulated p- and n-FETs (see C−F bond-induced dipoles in CYTOP). Voltage transfer characteristics (V_{IN}−V_{OUT}, solid line) and power consumption (dashed line) of hetero-CMOS (f) before and (g) after CYTOP encapsulation as obtained under various supply voltages (V_{DD} values) ranging from 1 to 5 V. (h) VTC and its mirror reflection of hetero-CMOS shows low and high noise margins (NM_L and NM_H) as obtained under V_{DD} = 5 V.

transition voltage (−2 V); it remains as a serious problem resulting in V_{IN}−V_{OUT} signal mismatch in NOT gate, invalidating any logic function. This originates from the fact that our two FETs are in depletion mode. To resolve this issue of V_{IN}−V_{OUT} signal mismatch, we attempted to fabricate another set of glass-substrate hetero-CMOS (Figure 4a) using little thinner p-WSe_2 and n-MoS_2 flakes (3.5 and 5.4 nm, respectively, in Figure 4b) for the channel along with a CYTOP passivation layer coating on CMOS devices (Figure 4c), in consideration that our back-gate FETs with thin flake channels may have a smaller number of carriers, which induce a threshold voltage shift in FETs.[13] Moreover, the organic CYTOP contains C−F bond-induced dipoles inside (see the dipole schemes in the inset FETs of panels d and e of Figure 4), which are supposed to induce more holes into thin p-WSe_2 and to reduce electrons in thin n-MoS_2, controlling their respective I_D current.[24] In addition, the device needs a top passivation layer anyway for ambient stability improvement. As a consequence, we could control the I_D current in p- and n-FETs, as shown in panels d and e of Figure 4; the 3.5 nm thin p-WSe_2 channel initially shows 0.2 μA (μ_{sat} = 0.1 cm^2 V^{-1} s^{-1} at V_D = −1 V, and μ_{lin} ~ 20 cm^2 V^{-1} s^{-1} at −0.1 V) but later 10 μA (μ_{sat}= 17 cm^2 V^{-1} s^{-1}, and μ_{lin} ~ 40 cm^2 V^{-1} s^{-1}) with a threshold voltage of ~0.5 V (as shown in Figure S5d) after CYTOP passivation, and in the opposite way, the 5.4 nm thin n-MoS_2 channel displays initial 20 μA (μ_{lin} = 22 cm^2 V^{-1} s^{-1}) and final 2 μA (μ_{lin} = 7 cm^2 V^{-1} s^{-1}) with a threshold voltage (V_{TH} ~ 2.9 V, as shown in Figure S5e) of an enhanced mode FET. Such thickness effects almost realize a positive transition voltage (~0.1 V) in our CMOS VTC curves of Figure 4f, but peak power consumption and voltage gain degrade somehow to be 100 nW and ~10, respectively. Noticeable improvement in the VTC behavior of the CMOS inverter actually came from CYTOP encapsulation, as shown in Figure 4g; positive transition voltage of 2.3 V (at 3−5 V of V_{DD}) was achieved along with a high voltage gain of 23 and ~1 nW peak power consumption. Moreover, an almost ideal noise margin[39] was obtained for much improved signal matching, as seen in Figure 4h, where NM_L = 0.385V_{DD} and NM_H = 0.495V_{DD}. We again attribute this type of success to the thickness modulation and CYTOP encapsulation, which could control the threshold voltage and I_D current as well, because we could finally achieve the enhanced mode n-MoS_2 FET without losing the mobility (or on-current I_D) value of WSe_2 and MoS_2 FETs. More details on the mobility plots and voltage gain curves are found in panels a−c and f−h of Figure S5, respectively. As a matter of fact, in typical complementary inverters, the transition voltage appears apparently proportional to the supply voltage (V_{DD}) because p- and n-channel FETs show quite a symmetrical behavior in output and transfer characteristics. Therefore, most

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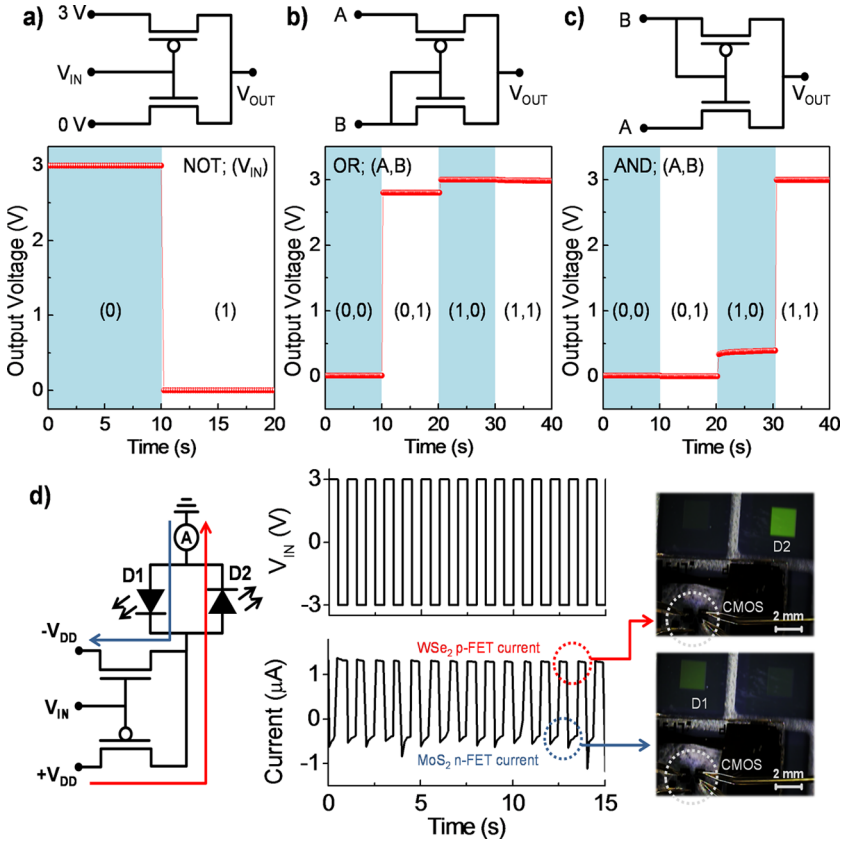

Figure 5. Schematic circuit diagrams and time domain V_{OUT} versus V_{IN} plots of (a) NOT, (b) OR, and (c) AND logic gates. Input logic (0) and (1) indicate the input voltages of 0 and 3 V, respectively. (d) Left circuit diagram describes a push−pull circuit comprised of hetero-CMOS inverter and two antiparallel OLEDs. Central plots show input voltage and output current curves at 10 Hz switching. Right snapshot images display the alternative switching of green OLEDs (D1 and D2) by n-MoS_2 and p-WSe_2 FETs.

ideal transition voltage would be $0.5V_{DD}$ according to load-line analysis. However, our case is quite deviated from ideal symmetry; the p-type WSe_2 transistor approaches to saturation behavior and shows ∼10 times higher mobility than that of our n-type MoS_2 transistor with linear output behavior. As a result, our inverter might behave as somewhat resistive-load (or depletion-load) type, which also shows proportionality but with a small increase of transition voltage, despite a large V_{DD} increase,[35,40,41] although our complementary-like inverter brought good power consumption and noise margin.

Logic Gates and Push−Pull Circuit Based on 2D Hetero-CMOS. On the basis of the above hetero-CMOS inverter with a positive transition voltage, two types of applications were implemented: basic logic operation (using pass transistor circuits)[42] and OLED switching. According to the respective plots of panels a, b, and c of Figure 5 for NOT, OR, and AND logics in the pass transistor circuits,[42] our hetero-CMOS circuits appear nicely operating when 0 and 3 V input voltages (V_{IN}) were applied for central, A, and B terminals (for NOT gate, V_{DD} = 3 V). More interesting may be the push−pull circuit of Figure 5d to alternatively switch two OLED pixels (D1 and D2). The alternative V_{DD} values of −3 and +3 V were dynamically supplied with 1−10 Hz square wave V_{IN} of ±3 V. Because the WSe_2 p-FET could supply a higher current as expected from Figure 4d, the corresponding OLED pixel (D2) appears brighter than the other pixel (D1), which is switched on by MoS_2 n-FET. For more details, 1, 5, and 10 Hz switching operations are demonstrated in a supporting AVI file (supporting video clip), while the device property of green OLEDs (courtesy of Samsung Display) is also shown as $I-V$ curves in Figure S6 for reference.

CONCLUSION

In summary, hetero-CMOS inverters with 2D semiconductor channel FETs of p-WSe_2 and n-MoS_2 have been successfully fabricated on both 285 nm thick SiO_2/p^+-Si and glass substrates using a direct imprinting method. Our hetero-CMOS inverters with bottom-gated p- and n-FETs well operate on both substrates, but they show much superior performances on glass because of gate patterning, electrical isolation between n- and p-FETs, and much reduced overlap capacitance: faster dynamic switching behavior, higher voltage gain of ∼27, and sub-nanowatt power consumption. Input−output signal mismatch, caused by negative transition voltage in the CMOS device, was resolved using thinner flake channels and CYTOP encapsulation, which result in both enhanced mode n-FET and a positive CMOS transition voltage. Our CMOS device with a patterned gate on a glass substrate well operates in the circuits of NOT, OR, and AND logic, also demonstrating a push−pull circuit for OLED pixel switching. We now conclude that our 2D hetero-CMOS inverter by a simple direct imprint method is quite useful and promising toward future nanodevice/electronic applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b06027.

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Table for published reports on 2D-CMOS, schematic images describing fabrication processes, gate voltage versus mobility plots, square root drain current versus gate voltage ($\sqrt{I_D}-V_{GS}$), and drain current versus gate voltage (I_D-V_{GS}) plots to obtain threshold voltages, drain current−drain voltage (I_D-V_{DS}) output curves, AFM result of the patterned Au/Ti gate on glass, voltage gain ($-dV_{OUT}/dV_{IN}$) plots of hetero-CMOS as a function of the input voltage, and current−voltage ($I-V$) curves of green OLED (PDF)
Supporting video clip (AVI)

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Notes

The authors declare no competing financial interest.

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